## AMENDMENTS TO THE SPECIFICATION

**IN THE SPECIFICATION**

Please amend the paragraph beginning on page 1, line 2, as follows:

--CROSS REFERENCES TO RELATED APPLICATIONS

This application is a divisional of U.S. Patent Application 09/566,916 filed on 9 May 2000, and claims priority under 35 U.S.C. 119 to Korean Application No. 99-16605, filed on 10 May 1999, and upon Korean Patent Application No. 00-3398, filed 25 January 2000, the contents of both of which are hereby incorporated by reference in its entirety for all purposes.--

Please replace the paragraph beginning on page 6, line 12 with the following rewritten paragraph:

--Then, as shown in Fig. 8, a first insulation layer 56 is formed over the entire surface of the resultant structure, and electrodes 58 and 60, which contact impurity diffusion regions 42 and 57 of the peripheral devices, are formed. A second insulation layer 62 is then deposited over the resultant structure. In Figs. 6 and 8, reference numeral 32 represents an N-well, reference numerals 46 and 50 represent capping layers, and reference numeral 52 represents spacers.--

Please replace the paragraph beginning on page 15, line 8, with the following rewritten paragraph:

--In Figs. 9 through 13, reference numeral 70 represents a semiconductor substrate, reference numeral 72 represents a buried impurity diffusion region,

reference numeral 74 represents a gate insulation layer, reference numeral 76 represents a grown insulation layer, reference numeral 78 represents a pad conductive layer, reference numeral 80 represents a word line (i.e., a gate), reference numeral 82 represents a gate protective insulation layer, reference numeral 84 represents a planarization layer, reference numeral 86 represents a metal interconnection, reference numeral 88 represents a metal interconnection protective insulation layer, reference numeral 89 represents a channel region of a cell, which requires programming and into which impurities are implanted to control the threshold voltage of channel regions. The word line 80 may be formed of two layers, a polysilicon layer 80a and a metal silicide layer 80b.--

On page 16, line 1, please amend the paragraph as follows:

--Cell isolation impurity layers 73 ~~Although not illustrated, cell isolation impurity layers~~ for enforcing the isolation between the cell transistors, are preferably formed in the regions of the buried impurity diffusion regiosn 72 that are not overlapped by the pad conductive layers 78.--